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USB-EPP Evaluation Kit

User Reference Manual

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1 Introduction

Philips USB-EPP Kit is a comprehensive kit offering you the opportunity to discover the full potential of Philips PDIUSBD12 (or D12). It also offers you the know-how on how to convert your existing EPP into USB devices. The kit comes with the D12, main (or evaluation) and daughter boards, test application program (or Applet), USB driver, and some sample firmware source codes.

D12 is a high performance USB interface device that offers not only DMA transfer capability, but also features for a cost-effective microcontroller-based system. This kit gives you the opportunity to perform a thorough evaluation of the capabilities and features of this device as well as to quickly and easily realize the technical know-how of converting your existing EPP devices such as the digital still camera, mass storage device, and scanner into USB devices. The daughter board, which is basically a simple memory board with EPP port interface, is used for emulating an EPP device such as an EPP scanner during the evaluation test.

With the Applet, you can operate the kit in three different modes: Print, Scan, and Loop back modes. The purpose for having the print and scan modes is to allow the evaluation board to emulate either the printer or scanner environment. The Loop back mode is to show you the integrity of the data when large data packet is sent and received from the host system.

Running the kit only requires a new generation PC (motherboard with USB port) with Microsoft Windows 98 operating system. The firmware provided with the Kit is written in C language, thereby allowing you to port it to any other platforms for compiling. With this kit, you can develop your USB devices through the firmware and hardware schematic.

2 SETTING UP THE USB-EPP EVALUATION SYSTEM

Setting up the USB-EPP evaluation system using the kit does not require a lot of effort. All that is needed to set up such a system is to simply connect the USB-EPP main and daughter boards to the host system as shown in Figure 2-1, and then install the software provided with the kit.

However, before you set up such a system, check to ensure that you have the following:

? Host system with USB motherboard or USB plug-in card;

? Microsoft Windows 98 operating system; and

? USB-EPP main and daughter boards, USB cable, and diskette provided with the kit.

Depending on your preference, you may need the optional RS-232 cable with a 9-pin Male and Female D-type connectors for the bus-powered mode and the AC-DC power adapter with +5V output for the self-powered mode.

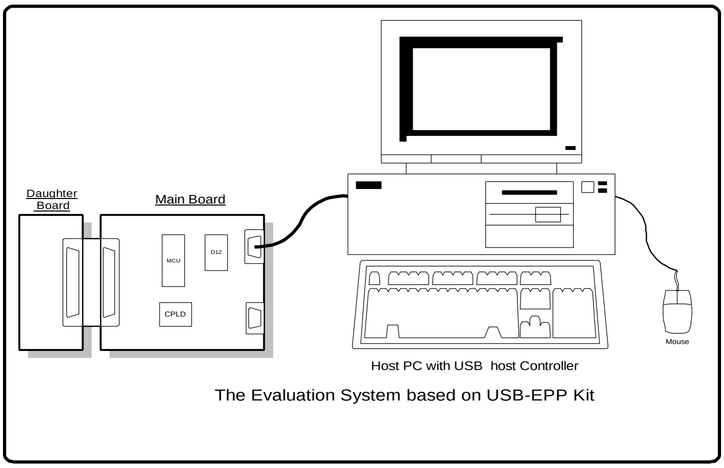

Daughter Board
Main Board
MCU
D12
CPLD
Mouse
Host PC with USB host Controller
The Evaluation System based on USB-EPP Kit

Figure 2-1: The USB-EPP Evaluation System

2.1 Installing the hardware

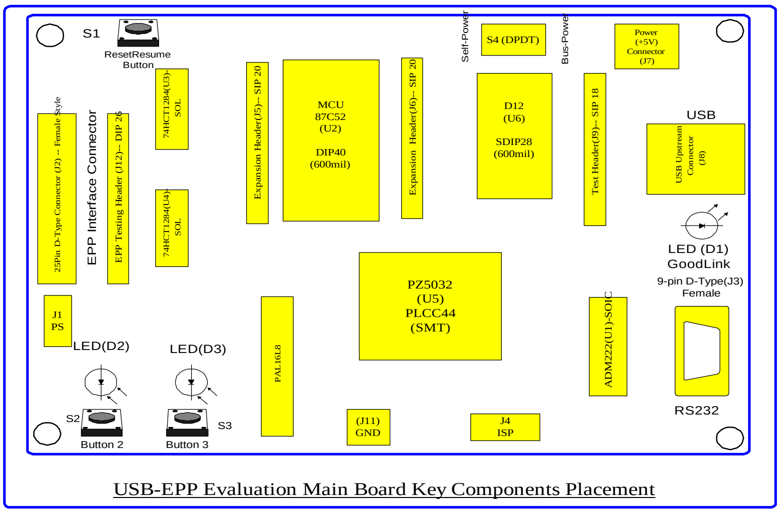


Figure 2-2: Locations of the components on the main board.

Figure 2-2 above shows you the various components located on the main board. For a detailed description of the various components, see “Hardware and Functional Overview”.

To install the hardware:

1. Make a backup copy of the original diskette provided with the kit.

2. Make sure that Pin 1 and Pin 2 of J1 are shorted by placing a jumper over them so that the daughter board is able to receive the power supply.

3. If the main board is used for connecting to EPP devices such as the scanner, then Pin 2 and Pin 3 of J1 must be shorted by placing a jumper over them.

4. Connect the daughter board to the main board through the 25-pin D-type connector.

5. If you are using the self-powered mode, you will need to provide 5 VDC supply to the power connector (J7) from an AC-DC power adapter with at least 500 mA output. Thereafter, flip the switch (S4) to the direction where “self-power” is labeled on the main board.

6. If you are using the bus-powered mode, flip the switch (S4) to the direction where “bus-power” is labeled on the main board.

7. Connect one end of the USB cable to the upstream connector (J8) on the main board and the other end to the host system or USB hub.

8. Once the USB cable is connected, follow the instructions on the screen to install the device driver.

2.2 Installing the software

The software responsible for controlling the hardware and ensuring that it works includes the firmware, the test application program (or the Applet), and the device drivers.

The firmware is already stored in the 87C52 microcontroller (OTP type). If you want to change the firmware or use your own firmware, all that you need to do is to remove the 87C52 microcontroller and replace it with your own microcontroller.

To install the Applet:

1. Insert the diskette into your disk drive.

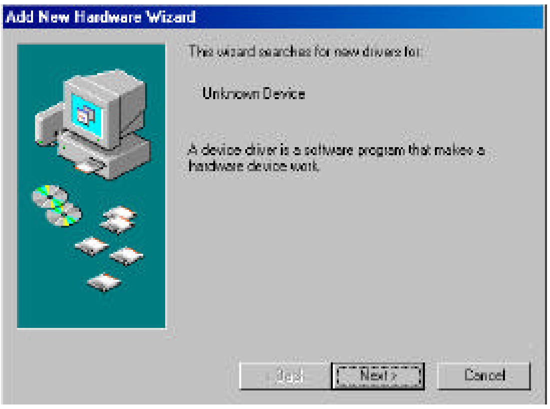
2. Copy the file D12TEST.EXE contained in the diskette to a directory of your choice such as C:\USBEPP.

3. Create a shortcut by dragging the file D12TEST.EXE from the directory to the desktop. An icon similar to Figure 2-3 appears.

Figure 2-3: The icon on the desktop.

To install the device drivers:

1. When you connect the USB cable to your host system for the first time, a dialog box similar to Figure 2-4 appears. Click the Next button.



Add New Hardware Wizard

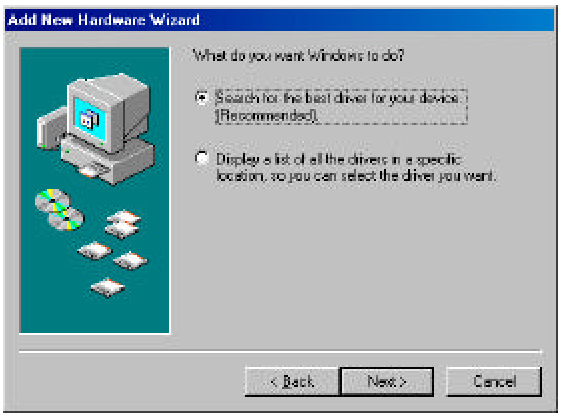
This wizard searches for new drivers for:

Unknown Device

A device driver is a software program that makes a hardware device work.

Figure 2-4

2. When a dialog box similar to Figure 2-5 appears, select the first item and click the Next button.



Add New Hardware Wizard

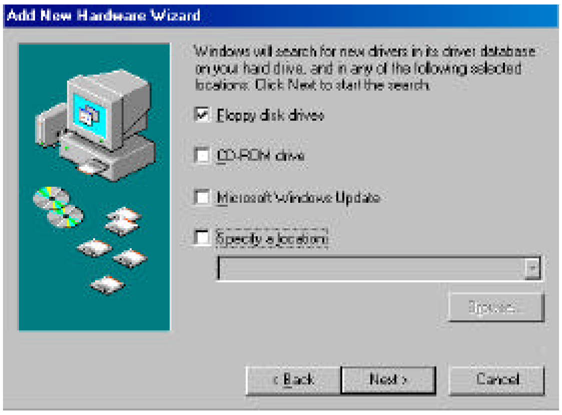
What do you want Windows to do?

● Search for the best driver for your device. (Recommended).

○ Display a list of all the drivers in a specific location, so you can select the driver you want.

Figure 2-5

3. When a dialog box similar to Figure 2-6 appears, select Floppy disk drives and click the Next button.



Add New Hardware Wizard

Windows will search for new drivers in its driver database on your hard drive, and in any of the following selected locations. Click Next to start the search.

☑ Floppy disk drives

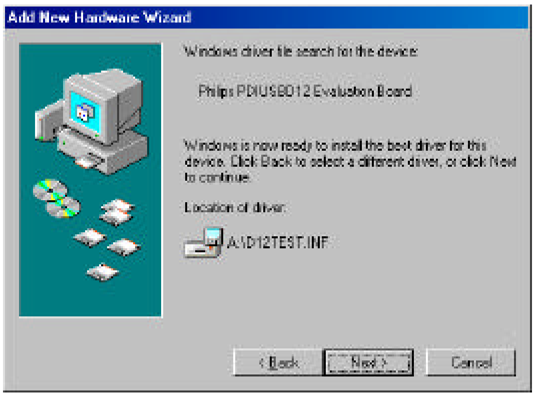
☐ CD-ROM drive

☐ Microsoft Windows Update

☐ Specify a location:

Figure 2-6

4. When a dialog box similar to Figure 2-7 appears, click the Next button.



Windows driver file search for the device:

Philips PDIUSBD12 Evaluation Board

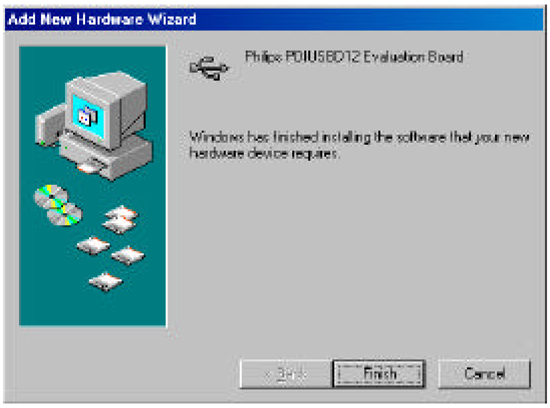
Windows is now ready to install the best driver for this device. Click Back to select a different driver, or click Next to continue.

Location of driver:

A:\D12TEST.INF

Figure 2-7

5. When a dialog box similar to Figure 2-8 appears, click the Finish button to end the installation.



Philips PDIUSBD12 Evaluation Board

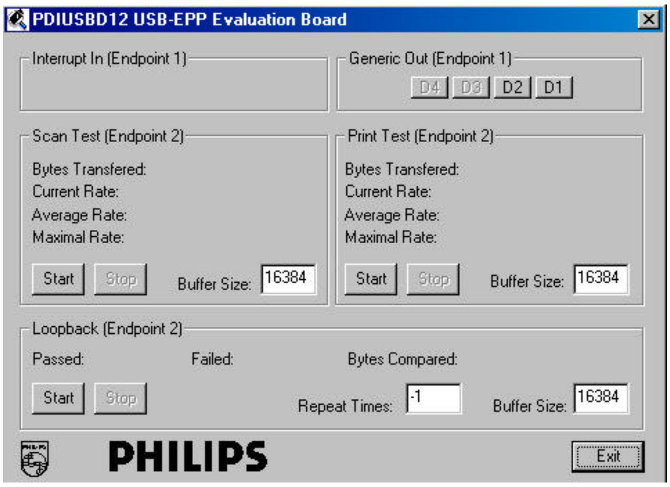
Windows has finished installing the software that your new hardware device requires.

Figure 2-8

2.3 Running the Applet

The Applet supports 3 different test modes: Print, Scan, and Loop back modes. The purpose for having the print and scan modes is to allow the evaluation board to emulate either the printer or scanner environment. The Loop back mode is to show you the integrity of the data when large data packet is sent and received from the host system.

To run the Applet, click on the D12Test.exe icon on your desktop. An interface similar to Figure 2-9 appears.



Buffer Size: 16384

Buffer Size: 16384

Repeat Times: -1

Buffer Size: 16384

Figure 2-9: The Applet.

2.3.1 Description of D12 Endpoint Configuration

The table below describes the PDIUSBD12 Endpoints configuration Mode 0.i.e. it is Non-Iso mode , the reset 3 mode (Isochronous mode) can be found on the D12 specification.

Endpoint Number	Endpoint Index	Transfer Type	Endpoint Type	Direction	Max Packet Size(Bytes)
0	0 1	Control Out Control In	Default	Out In	16 16
1	2 3	Generic Out Generic In	Generic Generic	Out In	16 16

2	4
	5
		Generic(Main) Out
		Generic(Main) In
			Generic
			Generic
				Out
				In
					64(another 64 for double buffer)
					64(another 64 for double buffer)

Table 2-1

2.3.2 Description of D12 Endpoints

The table below describes in detail the operations of the endpoints.

Endpoint Number	Endpoint Type	Operations
1	Generic In	This pipe is defined as Interrupt pipe. The USB-EPP evaluation board sends specific data packet to the host system when the test key is pressed or released.
1	Generic Out	This pipe is defined as Bulk Out pipe. Data packet received from the host system is interpreted as LED control, and the firmware will light up the corresponding LED.
2	Main In Main Out	These pipes are defined as Bulk In/Out endpoints. The Applet and the evaluation board support 3 test modes: loop back, print, and scan modes.

Table 2-2

The Generic In and Generic Out endpoints have a maximal packet size of 16 bytes, and thereby make them suitable for devices that require small size data transfer such as the keyboard, mouse and logic controls. The main endpoints have a maximal packet size of 64 bytes (for Bulk/Isochnorous mode) or 128 bytes (for Isochnorous mode) with double buffering capacity. Hence, they are suitable for high data rate and large size data transfer.

Three different test modes are supported on the main endpoints. They are as follows:

? Scan mode: In this mode, the evaluation board emulates the scanner environment. This mode is used to evaluate the maximal Bulk In transfer rate.

? Print mode: In this mode, the evaluation board emulates the printer environment. This mode is used to evaluate the maximal Bulk Out transfer rate.

? Loop back mode: In this mode, the evaluation board receives data packets from the Main Out endpoint (Endpoint Index 4) and sends them back to the host system from the Main In endpoint (Endpoint Index 5). This mode is used to test the firmware’s ability to control the data flow and the integrity of data transfers.

Since the firmware is protocol-based, the host system can inform the firmware to set any possible modes. There is therefore no longer any need to physically set the scan test mode before running the scan test on the firmware running on the evaluation board. Please refer to 4.8.1 for more information on the protocol-based transfer. Please refer to the section “DMA Support” for more information on the protocol-based transfer.

The “buffer size” of the Applet is the size of the data buffer, which the Applet passes to the USB system drivers for receiving or transmitting. It is therefore the responsibility of the USB system drivers to divide them into smaller data packets e.g. 64 bytes for bulk transfer. The maximal buffer size is limited by the USB system drivers. Best transfer rate over USB can be achieved by optimizing the buffer size.

The buffer size in loop back test mode is also limited by the USB-EPP DMA burst transfer size (DMA_BTS register of CPLD is only 14bits i.e. 16kbytes) on the device side. As in the DMA mode, CPLD needs to generate the EOT_N signal to D12 when the DMA is receiving and transmitting the maximal buffer size, which is determined by the CPLD internal register DMA_BTS. Since the daughter board has 512 Kbytes SRAM, it would need to store 16 Kbytes into 32 blocks of memory. The default buffer size (maximal size in DMA mode) for loop back test is 16384 bytes. If the infinite loop back mode is to be used, “-1 “ should be set the in the Repeat Times box.

3 Hardware and Function Overview

3.1 Main Board Block Diagram

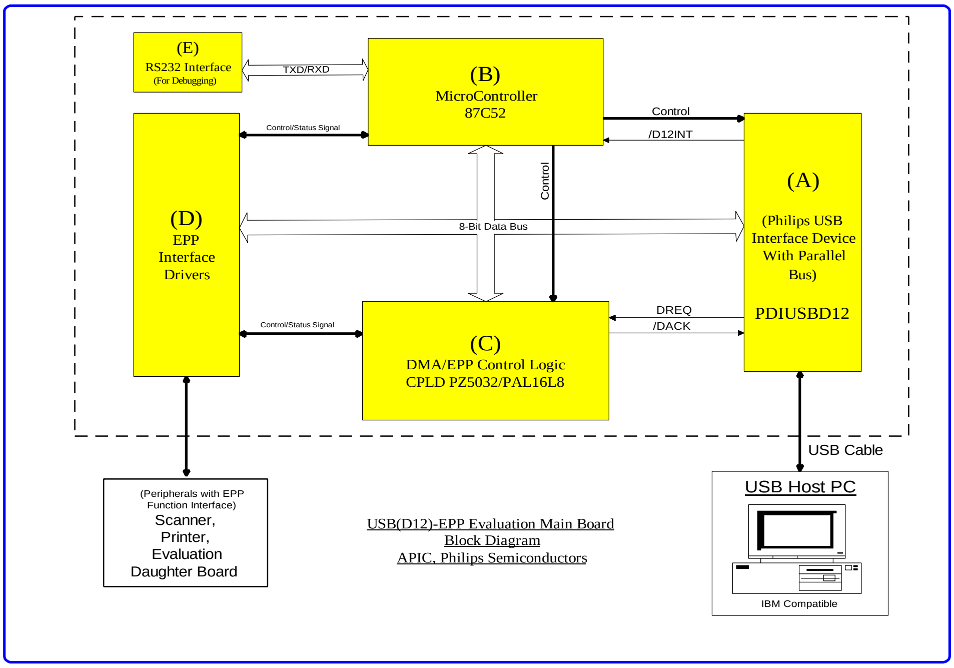


Figure 3-1: The main board block diagram.

There are 5 elements on the main board. The board has three interfaces. They are the USB interface that is connected to the host system, the EPP interface that is connected to peripherals such as printer and scanner, and the RS232 interface that is connected to the host system for firmware debugging only.

Element (A) is a Philips PDIUSBD12 USB interface device. It implements all the functions of the USB device, and has an 8-bit parallel data bus for Microcontroller (B) or DMA accessing (C).

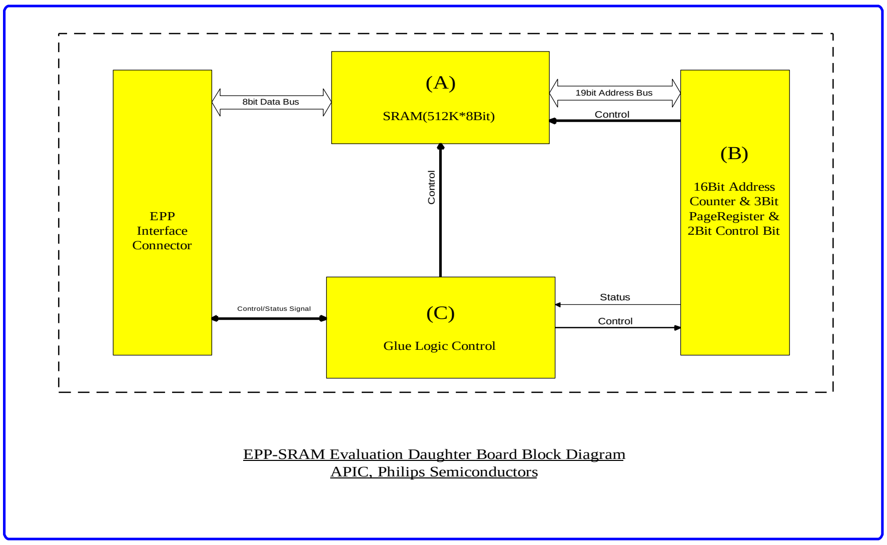
Element (B) is a Microcontroller. It is a member of the 8051-family. The Philips 87C52 is used here. It implements USB enumeration, EPP negotiation, D12 Interrupt service, DMA transfer management, and RS232 port monitoring .

Element © is the DMA and EPP control logic. It is implemented by CPLD (Philips PZ5032) and PAL16L8. This element supports D12 DMA and EPP accessing timing as well as a built-in 14-bit counter for DMA burst control.

Element (D) performs only a pure buffering function for EPP interface. It consists of 2pcs 74HCT1284.

Element (E) is an RS232 buffer (ADM222). The host system can communicate with the Microcontroller through this RS232 port.

3.2 Daughter Board Block Diagram



EPP-SRAM Evaluation Daughter Board Block Diagram
APIC, Philips Semiconductors

Figure 3-2: The daughter board block diagram.

There are 3 elements on the daughter board. It contains the EPP interface which is for connecting to peripherals such as the printer and scanner and the RS232 interface which is for connecting to the host system for firmware debugging.

Element (A) is an SRAM (512K*8bit) for the main board to store the data so that it can emulate the printer for receiving data (data pool) or the scanner for transmitting data (data source).

Element (B) includes a 14-bit counter, a 5-bit SRAM page switching, and a 2-bit control register.

Element (C) includes the decoding logic, which meets the EPP logic and timing requirement.

3.3 Description of CPLD State Machine

The Figure(bubble diagram) below describes the DMA state machine of the CPLD . For DMA reading from D12 to EPP interface there are 7 states for the state machine, i.e. they are IDLE/DMAREAD1/ DMAREAD2/DMAEND/DMAEND1/DMAEND2/DMAEND3 and forFor DMA reading from EPP interface and writing to D12 there are also 7 states for the state machine, i.e. they are IDLE/ DMAWRIT1/ DMAWRIT2/DMAEND/DMAEND1/DMAEND2/DMAEND3 . Two states are different and the reset states can be shared by DMA-read or DMA-write.

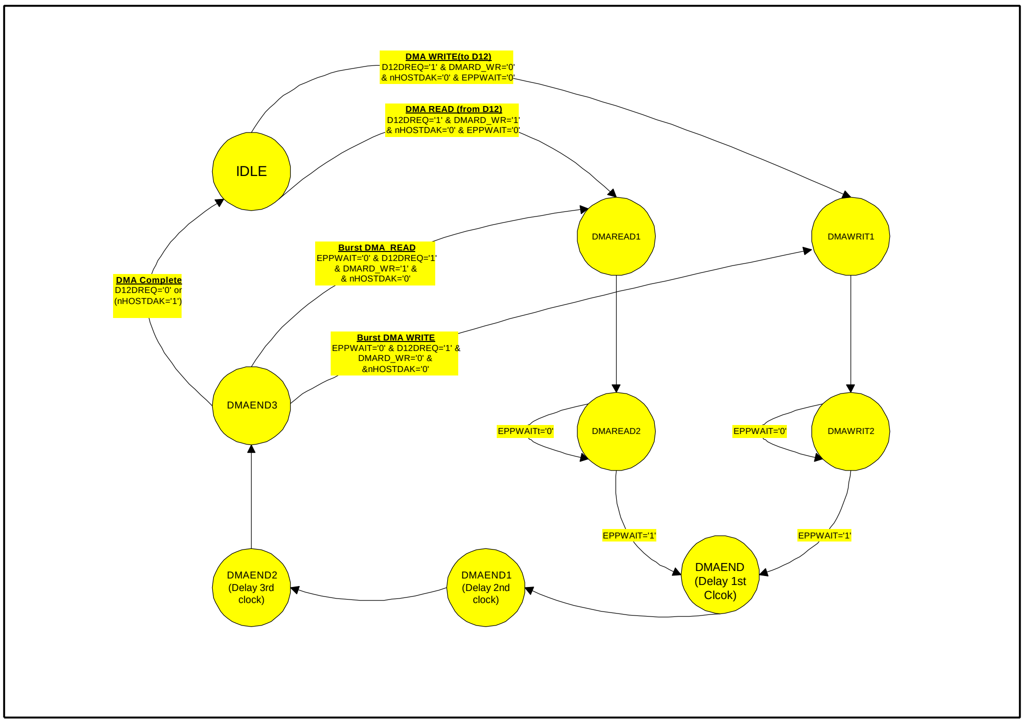


Figure 3-3: The flow diagram of the EPP and DMA Controller (CPLD) State

3.4 Description of Registers

3.4.1 Address Mapping of CPLD Internal Registers and D12 Registers

MCU External Memory Address A1,A0 (Latched from D1 and D0)	Read/Write	Register Description D7-D0 (8-Bit)	After Reset (Default value)
00	R/W	DMA_BTS (7:0), Counter Low DMA Burst Transfer Size, Lower 8-Bit	0x00
01	R/W	DMA_BTS(13:8) Counter high DMA Burst Transfer Size, Upper 6-Bit (Bit-7 and Bit-6 are don't care????)	0x00
10	R/W	PDIUSBD12 Data Register (See D12 Data Spec.)	See Philips PDIUSBD12 Spec.
11	R/W	PDIUSBD12 Command Register (See D12 Data Spec.)	See Philips PDIUSBD12 Spec.

Table 3-1: The address mapping of CPLD and D12.

DMA_BTS is a 14-bit register, which can be accessed by MCU (87C52). It can be divided into two registers, the lower 8-bit (address 0x0) and upper 6-bit (address 0x1). Once you access this 14-bit register, you need to access it twice (addresses 0x0 and 0x1) because the data bus is only 8-bit wide.

This register (counter) is used in the USB device D12 DMA transfer mode. Before D12 starts the DMA transfer (DMA reads from D12 and writes to EPP or DMA reads from EPP and writes to D12), MCU needs to set the DMA burst transfer size (Block size) to CPLD (U5) DMA_BTS register.

During the DMA mode, DMA_BTS register can be automatically decreased to ONE when one transaction (one read/write accessing) has been done. When this register reaches ZERO, it immediately generates a DMA EOT (End of Transfer) signal (active low) to D12, stops DMA request, then finishes DMA transfer and clear the internal Endpoint.

Notice that before DMA starts, MCU needs to set DMARD_WR to 1 (DMA reads from D12 mode) or 0 (DMA writes to D12 Mode). Otherwise, DMA controller will get the wrong DMA direction transfer.

3.4.2 Description of the Daughter Board's Registers

3.4.2.1 Control and Page Selection Register (CTRL_PAGE)

CTRL_PAGE register is used to set the SRAM page number (ADR18-ADR14), clear ADDRCNTR, and preset the starting address for the SRAM. Altogether there are 32 pages for the SRAM page switching. Each page is 16 Kbytes (ADR13-ADR0) in size, which is restricted by the CPLD internal DMA burst transfer size register. It is has the same size as ADDRCNTR.

Bit: CLEAR: After reset, the default value is 0. When MCU writes 2-byte data to the address register (/ASTROBE active), that is Bit 7 (CLEAR) is set to 1 first and then reset to 0 (positive pulse), the ADDRCNTR should be cleared to 0. When accessing the SRAM address from 0x00000, you need to perform the CLEAR operation.

Bit: CNTRINC: After reset, the default value is 0. If you want to make ADDRCNTR to increase automatically to one after accessing the SRAM (read or write, /DSTROBE active), this bit should be set to 0. Otherwise, the ADDRCNTR output will stop increasing. You can also use this bit to set the start SRAM address. First, use the CLEAR operation, write 1, and then 0 to Bit 6 (this bit) of the EPP Address register (/ASTROBE active). The ADDRCNTR should increase to one so that you can get the address you want by controlling the loops by setting Bit 6 to 1 and 0.

Bit: ADR18-ADR14: After reset, the default value is B"00000", which is the page number pointed to the SRAM (512K*8bit). The maximum pages are 32, that is, from 0 to 31. Note that the CTRL_PAGE setting is controlled by /ASTROBE signal and not by /DSTROBE on the EPP interface.

Bit	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Function	CLEAR	CNTRINC	ADR18	ADR17	ADR16	ADR15	ADR14	X
Default	0	0	0	0	0	0	0	0

Table 3-2: The description of CTRL_PAGE.

3.4.2.2 14-Bit Address Counter (ADDRCNTR)

The ADDRCNTR register is used as an address register on the daughter board, which points to SRAM (512K*8Bit), together with the Page setting ADR18-ADR14 in the CTRL_PAGE register. After reset, the default value is 0x00000. This register can also be controlled by the CLEAR and CNTRINC registers.

Bit	Bit13-Bit0	Default Value
Function	ADR13-ADR0	B"00000000000000"

Table 3-3. The description of ADDRCNTR.

3.5 Signals description in the EPP Mode

The signal used for the EPP mode transfer are described in detailed in clause 5 of IEEE std 1284 -1994 . they are summarized in the table below.

Compatibility Mode Signal Name	**EPP Mode Signal Name**	**EPP Mode Signal Description**
nStrobe	nWrite	Set low to denote an address or data write operation to the peripheral. Set high to denote an address or data read operation from the peripheral
Data1 … Data 8	AD1 … AD8	Host –to-peripheral or peripheral-to-host address or data
nAck	Intr	Used by the peripheral to interrupt the host , This signal is active high and positive edge triggered.
Busy	nWait	This signal should be driven inactive as a positive acknowledgement from the peripheral that transfer of data or address is completed. The signal is active low. It should be driven active as an indication that the device is ready for next address or data transfer.
nAutoFd	nDStrb	This signal is active low, it is used to denote a data cycle.
NInit	nInit	This signal is active low. When driven active(low), this signal initiates a termination cycle that results in the interface returning to compatibility Mode.
nSelectIn	nAStrb	This signal is active low. It is used to denote an address cycle. It is active low.
PError	User defined 1	This signal is manufacturer specific and beyond the scope of IEEE standard
nFault	User defined 2	This signal is manufacturer specific and beyond the scope of IEEE standard
Select	User Defined 3	This signal is manufacturer specific and beyond the scope of IEEE standard

Table 3-4: The signal description of EPP Mode.

Four operation are supported on EPP mode:

a). Address Write b). Data Write

c). Address Read d). Data Read

3.6 Miscellaneous

? Press-Button S1—Reset or Resume the system

? Press-Button S2—PIPE testing

? Press-Button S3—PIPE testing

? LED D1—USB interface GoodLink indicator. When it is on, it means that the linking between USB host and USB device has been set up and enumeration has been done. If it is blinking, it means that data is being transmitted or received

? LED D2—PIPE testing

? LED D3—PIPE testing

? +5V Power Connector—DC 5V Input for USB self-powered, internal pole is 5V

? Power Supply Switch S4—Self-powered or Bus-powered switch. If no DC5V input provided, then it is used for Power-off or Bus-Powered

? Ground header J11—Connected to Ground for header testing

4 . APPENDIX

4.1 Appendix A:

Placement of the Components of Main/Daughter Board

Figures 4-1 and 4-2 show the locations of the components on the main and daughter boards, the physical dimension and the drilling holes, and pin layout of the IC. The dimensions of the main and daughter boards are 5.3” x 4.25” and 1.75” x 4.25” respectively. The total dimension of both boards is 7.05”x 4.25”.

The main components are as follows:

? U0: PAL16L8 programmable logic device

? U1: ADM222 CMOS RS232 driver/receiver

? U2: Micro-Controller 87C52

? U3/U4: IEEE1284 interface buffer, 74HCT1284

? U5: CPLD (PZ5032)

? U6: USB Device interface (PDIUSBD12)

? U7/U8: 74HCT393, Dual 4-bit Binary Ripple Counter

? U9: 512K*8bit SRAM, KM684000ALG

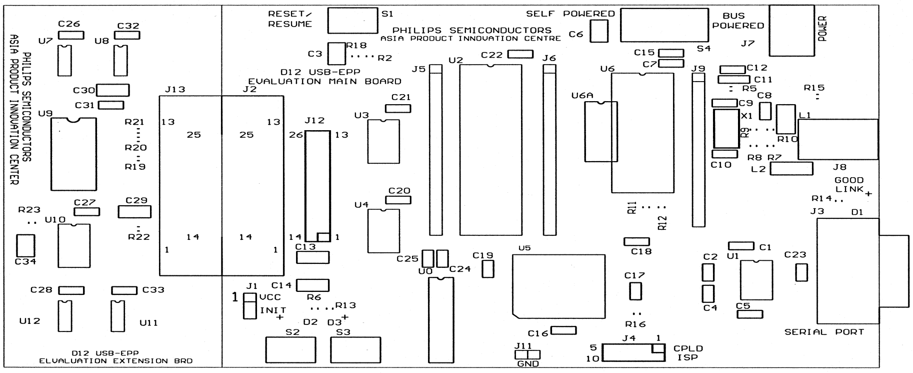


Figure 4-1: The top silk screen layer of the main/daughter board

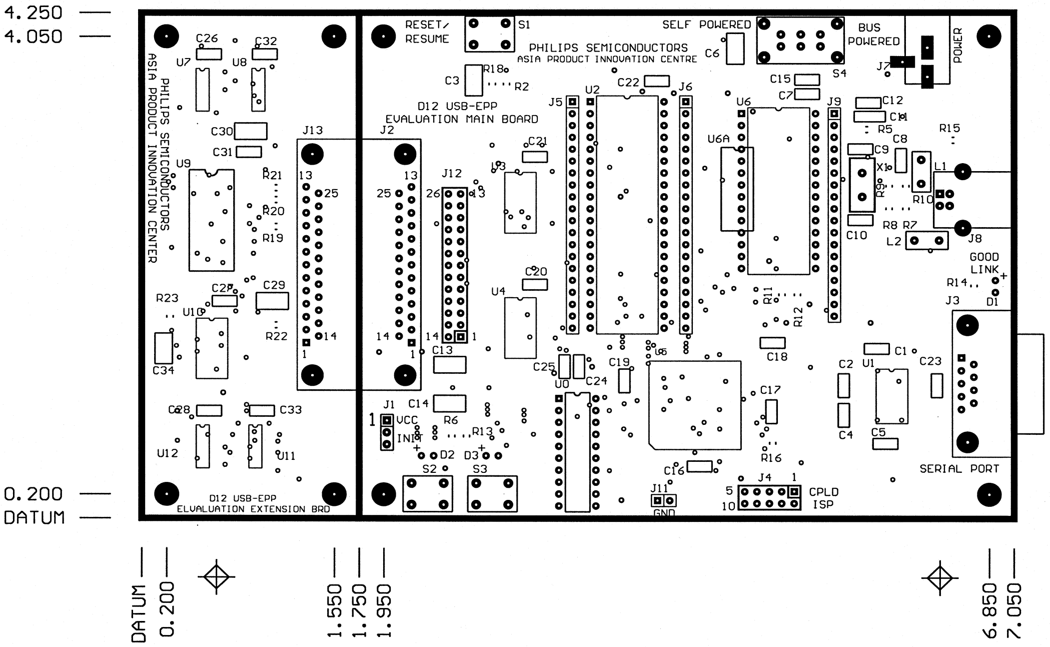


Figure 4-2: The top silk screen overlays with top solder mask layer of the main/daughter board.

4.2 Appendix B: Descriptions of the Connectors and Jumpers

For the locations of the various connectors and jumpers on the main and daughter boards, please refer to Figures 3-3 and 3-4. The following tables give you detailed information on the connectors and jumpers.

4.2.1 Microcontroller Connectors J5 and J6

The expansion connector J5 is connected from Pin1 to Pin 20 of the MCU (Micro-Controller Unit). The expansion connector J6 is connected from Pin 21 to Pin 40 of the MCU. The purpose of having these connectors is to allow you to use MCU of other make through a pin converter. What you need to do is to build another small PCB of the same layout and pin definition as connectors J5 and J6. Also, it allows you to debug signal lines from CPLD and PAL devices.

Connector Name	**Pin No.**	**Signa Name**	**Signal Type**	**Description**
J5	1 (Square Pin)	/WRITE	I/O	EPP Write, Active Low
J5	2	/DSTROBE	I/O	EPP Data Strobe, Active Low
J5	3	/ASTROBE	I/O	EPP Address Strobe, Active Low
J5	4	WAIT	I	EPP Wait, Active High
J5	5	/INTR	I	EPP Interrupt, Active Low
J5	6	PE	I	Paper End

J5	7	/ERROR	I	ERROR, Active Low
J5	8	SELECT	I	Select Device
J5	9	MCURST	I	MCU Reset , Active High
J5	10	S232RXD	I	RS232 RXD
J5	11	S232TXD	O	RS232 TXD
J5	12	/D12INT	I	D12 Interrupt, Active Low
J5	13	SUSPEND	I	Suspend Mode
J5	14	RLED0	O	Red LED 0
J5	15	RLED1	O	Red LED 1
J5	16	/MCUWR	I/O	MCU Write to External Memory, Active Low
J5	17	/MCURD	I/O	MCU Read from External Memory, active Low
J5	18	MCUX2	O	Crystal
J5	19	CLK12M	O	Clock Output
J5	20	GND	Power	Ground

Table 4-1: The signal description of J5.

Connector Name	**Pin No.**	**Signal Name**	**Signal Type**	**Description**
J6	1 (Square pin)	VCC	Power	+5V
J6	2	D0	I/O	Micro-Controller Data Bus
J6	3	D1	I/O	Micro-Controller Data Bus
J6	4	D2	I/O	Micro-Controller Data Bus
J6	5	D3	I/O	Micro-Controller Data Bus
J6	6	D4	I/O	Micro-Controller Data Bus
J6	7	D5	I/O	Micro-Controller Data Bus
J6	8	D6	I/O	Micro-Controller Data Bus
J6	9	D7	I/O	Micro-Controller Data Bus
J6	10	VCC	Power	+5V
J6	11	ALE	O	Address Latch Enable, Memory mode
J6	12	/PSEN	I	Program Store Enable, Active Low means External Memory
J6	13	ALE1	O	Address Latch Enable, I/O Mode
J6	14	SWM0	I	Switch Mode 0
J6	15	SWM1	I	Switch Mode 1
J6	16	DMARD_WR	O	DMA Transfer Direction, Read from D12 / Write to D12

J6	17	WH ICH_PW	I	Bus Power (High) or Self-power (Low)
J6	18	/EPPINIT	O	EPP Initialization
J6	19	/HOSTDACK	O	Host DMA Acknowledgment
J6	20	HOSTDREQ	I	Host DMA Request

Table 4-2: The signal description of J6.

4.2.2 *Test Header J9*

The J9 test header for D12 USB interface device is used to detect/probe D12’s signals other than the data bus. However, the data bus can be detected from J6. Some signals of CPLD are also connected to this test header.

Connector Name	**Pin No.**	**Signal Name**	**Signal Type**	**Description**
J9	1(Square Pin)	D12A0	I	Address A0
J9	2	+3V3	Power	3.3V Power Supply
J9	3	D12DP	I/O	USB Data Plus Line
J9	4	D12DM	I/O	USN Data Minus Line
J9	5	VCC	Power	+5V
J9	6	XTAL2	O	Crystal
J9	7	XTAL1	I	Crystal
J9	8	GOODLNK	O	Good Link for the USB Interface Data Link Status
J9	9	VCC	Power	+5V
J9	10	/D12EOT	I	End of DMA Transfer
J9	11	/D12DACK	I	DMA Acknowledge
J9	12	D12DREQ	O	DMA Request
J9	13	/D12WR	I	IO Write to D12
J9	14	/D12RD	I	IO read to D12
J9	15	/D12INT	O	D12 Interrupt Out
J9	16	CLK12M	O	D12 Clock Output for Other Device
J9	17	SUSPEND	I/O	Suspend Output or Input
J9	18	/D12CS	I	D12 Chip Select

Table 4-3: The signal description of J9.

4.2.3 ISP Connector J4

This 10-pin connector is used for CPLD In System Programming(ISP) if PZ5032CS10A44 is used (ISP version) otherwise it is not useful for PZ5032-7A44(Non ISP version).Anyway if you don't have a CPLD programmer, you need only to use this connector for programming U5 CPLD directly. Philips provides the programming cable, which connects J4 to the PC parallel port. More information can be obtained from the Website: http://www.coolcpld.com

Connector Name	**Pin No.**	**Signal Name**	**Signal Type**	**Description**
J4	1(Square Pin)	GND	Power	Ground
J4	2	GND	Power	Ground
J4	3	NC	Not connected	
J4	4	GND	Power	Ground
J4	5	NC	Not connected	
J4	6	CPLDTCK	I	JTAG, TCK
J4	7	CPLDTMS	I	JTAG, TMS
J4	8	CPLDTDI	I	JTAG, TDI
J4	9	CPLDTDO	O	JTAG,TDO
J4	10	NC	Not Connected	

Table 4-4: The signal description of J4.

4.2.4 USB Serials-B Connector J8 (Upstream)

J8 connector is a standard USB serial B connector that has two data lines, V-Bus and Ground. The connector can be connected to the system directly or any USB hub downstream port. More details can be found in the USB specifications

ConnectorName	**Pin No.**	**Signal Name**	**Signal Type**	**Description**
J8	1(Square pin)	V_BUS	Power ,	+5V
J8	2	D-	I/O	Data Minus Line,
J8	3	D+	I/O	Data plus Line
J8	4	GND	Power	Ground

Table 4-5: The signal description of J8.

4.2.5 RS232 Interface Connector J3

The RS232 connector is used for debugging. It can be connected to the PC for monitoring the status of the D12 device. Only two signals are used, that is, signal to receive data and signal to transmit data. The debugging feature is as such. MCU will print all activities related to the USB specifications to any PC terminals. This feature allows developers to trap any failure especially in the enumeration process.

Connector Name	**Pin No.**	**Signal Name**	**Signal Type**	**Description**

J3	1(Square Pin)	NC	No Connected	
J3	2	RS232TXD	O	RS232 Transmit Data Line
J3	3	RS232RXD	I	RS232 Receive Data Line
J3	4	NC	Not Connected	
J3	5	GND	Power	Ground
J3	6	NC	Not Connected	
J3	7	NC	Not Connected	
J3	7	NC	Not Connected	
J3	9	NC	Not Connected	

Table 4-6: The signal description of J3.

4.2.6 Jumper J1

The jumper J1 is for supplying power (5V) to the daughter board and to allow you to connect to other EPP devices.

Jumper Name(J1)	Pins Connections	Description
CASE 1	Pin 2 connected to Pin 1 (short together by Jumper block)	Pin 1of Jumper J1 is VCC. Pin 2 is connected to Pin 16 (/INIT) of Connector J2 or Pin 16 of connector J13. For the daughter board, Pin 16 of J3 is supposed to have 5V. In this case (for connecting the daughter to the main board), Pin 2 and Pin 1 must be enabled.
CASE 2	Pin 2 connected to Pin 3 (short together by Jumper block)	Pin 2 of Jumper J is connected to Pin 16 of Connector J2, and J3 is connected to Pin 14 of U4 (/PINIT). If the main board needs to be connected to the EPP interface, Pin 2 and Pin 3 of J1must be enabled.

Table 4-7: The pin configurations of J1.

4.2.7 Parallel Port connector and its test header

The signal for the connectors J2 (female-type on main board), J13 (male-type on daughter board), and J12 (test header) is in full compliance with the IEEE Standard 1284-1994. J2 and J13 are D-type 25-pin female/male connectors while J12 is a 26-pin header for debugging.

ConnectorName	**Test Header Name**	**Pin No.**	**Signal Name**	**Signal Type**	**Description**
J2/J13	J12	1	/STROBE	O	Strobe D7-D0
J2/J13	J12	2	PD0	I/O	Data bus
J2/J13	J12	3	PD1	I/O	Data bus
J2/J13	J12	4	PD2	I/O	Data bus

J2/J13	J12	5	PD3	I/O	Data bus
J2/J13	J12	6	PD4	I/O	Data bus
J2/J13	J12	7	PD5	I/O	Data bus
J2/J13	J12	8	PD6	I/O	Data bus
J2/J13	J12	9	PD7	I/O	Data bus
J2/J13	J12	10	/ACK	I	Acknowledgment, May trigger Interrupt
J2/J13	J12	11	BUSY	I	Busy, Printer Busy
J2/J13	J12	12	PE	I	Paper End, Empty (Out of Paper)
J2/J13	J12	13	SELECT	I	Printer selected (On-line)
J2/J13	J12	14	/AUTOFD	O	Generate automatic line feeds after carriage returns
J2/J13	J12	15	/ERROR	I	Error
J2/J13	J12	16	/INIT	O	Initialize
J2/J13	J12	17	/SELECTIN	O	Select device
J2/J13	J12	18	GND for J2, NC for J12	Power	Ground
J2/J13	J12	19	GND for J2, NC for J12	Power	Ground
J2/J13	J12	20	GND for J2, NC for J12	Power	Ground
J2/J13	J12	21	GND for J2, NC for J12	Power	Ground
J2/J13	J12	22	GND for J2, NC for J12	Power	Ground
J2/J13	J12	23	GND for J2, NC for J12	Power	Ground
J2/J13	J12	24	GND for J2, NC for J12	Power	Ground
J2/J13	J12	25	GND for J2, NC for J12	Power	Ground
	J12	26	GND	Power	Ground

Table 4-8: The signal description of J2, J13, and J12.

4.2.8 IEEE1284-A Connector description

IEEE 1284 defines five communication modes. It uses the terms FORWARD CHANNEL to refer to the transfer from the host to the peripherals and REVERSE CHANNEL to refer to the transfer from the peripheral to the host. The five modes are Compatibility, Nibble, Byte, EPP, and ECP.

With so many modes to choose from, the host and peripheral need to decide which mode they intend to use to communicate to one another. IEEE 1284's negotiation phase enables devices to talk back and forth so that they can decide on the best mode to use. Through negotiating, the host can find out which mode would be supported by the peripheral. If a peripheral supports multiple modes, the negotiation will inform the peripheral which mode the host wishes to use.

For the purposes of this evaluation kit, we have pre-selected the Enhanced Parallel Port (EPP) mode so that data is transferred at a higher speed in both directions. EPP can distinguish between two types of information, which is usually defined as data and addresses. In the EPP mode, there are only 2 types of information. They are data and address transfer.

The table below shows the pin numbers and their assigned signal names for the IEEE1284 –A connectors. The 1284-A connector is a 25-pin subminiature D-shell connector.

Pin #	Source	Compatibility mode	Nibble mode	Byte Mode	EPP Mode	ECP Mode
1	H	nStrobe	HostClk	HostClk	nWrite	HostClk
2	Bi-Dir	Data Bit1(LSB)	Data Bit1(LSB)	Data Bit1(LSB)	Address/Data Bit1	Data Bit1(LSB)
3	Bi-Dir	Data Bit2	Data Bit2	Data Bit2	Address/Data Bit2	Data Bit2
4	Bi-Dir	Data Bit3	Data Bit3	Data Bit3	Address/Data Bit3	Data Bit3
5	Bi-Dir	Data Bit4	Data Bit4	Data Bit4	Address/Data Bit4	Data Bit4
6	Bi-Dir	Data Bit5	Data Bit5	Data Bit5	Address/Data Bit5	Data Bit5
7	Bi-Dir	Data Bit6	Data Bit6	Data Bit6	Address/Data Bit6	Data Bit6
8	Bi-Dir	Data Bit7	Data Bit7	Data Bit7	Address/Data Bit7	Data Bit7
9	Bi-Dir	Data Bit8(MSB)	Data Bit8(MSB)	Data Bit8(MSB)	Address/Data Bit8	Data Bit8(MSB)
10	P	nAck	PtrClk	PtrClk	Intr	PeriphClk
11	P	Busy	PtrBusy	PtrBusy,	nWait	PeriphAck
12	P	PaperEnd	AckDataReq	AckDataReq,	User Defined Bit 1	nAckReverse
13	P	Select	XFlag	XFlag,	User Defined Bit 3	Xflag
14	H	nAutoLF	HostBusy	HostBusy	nDstrb	HostAck
15	P	nFault	nDataAvail	nDataAvail	User Defined Bit 2	nPeriphReq
16	H	nInit	nInit	nInit	nInit	nReverseReq
17	H	nSelectIn	1284Active	1284Active	nAstrb	1284Active
18		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground
19		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground
20		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground
21		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground
22		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground
23		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground
24		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground
25		Signal Ground	Signal Ground	Signal Ground	Signal Ground	Signal Ground

Table 4-9: The signal description of IEEE 1284-A.

4.3 Appendix C:

Main and Daughter Board Schematics

4.3.1 Main Board Schematic

The schematic for the main board, which is drawn on the OrCAD V7.0 EDA platform, is shown in Figure 4-3.

4.3.2 Daughter Board Schematic

The schematic for the daughter board, which is drawn on the OrCAD V7.0 EDA platform, is shown in Figure 4-4.